



Serial no. 10/614,928

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

SUBJECT: Serial #: 10/614,928
 File Date: July 8, 2003
 Inventor: Jin-Yuan Lee
 Examiner: Menz, Douglas M.
 Art Unit: 2891
 Title: "A STRUCTURE OF HIGH PERFORMANCE COMBO
 CHIP AND PROCESSING METHOD"

DECLARATION UNDER 37 CFR 1.131

Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

I, Jin-Yuan Lee, hereby state:

1. I am the inventor of Claims 25-45 of the above-identified patent application.
2. Prior to Dec. 4, 2000, I conceived of the idea for the electronic package as described and claimed in my application, and a copy of the invention disclosure describing my invention entered the United States of America before Dec. 4, 2000. The invention disclosure including drawings shows my invention as claimed in Claims 25-29, 31-35, and 45 and is attached as Exhibit A. Each of the dates blanked out from Exhibit A is prior to Dec. 4, 2000.

3. A first draft of the patent application was sent to me by George O. Saile & Associates on September 18, 2000. A copy of the letter accompanying the draft is attached as Exhibit B.
4. A second draft of the patent application was sent to me by George O. Saile & Associates on Dec. 8, 2000. A copy of the mail log of George O. Saile & Associates for Dec. 8, 2000 is attached as Exhibit C.
5. I returned the second draft of the patent application to George O. Saile & Associates. A copy of their mail log shows the draft was received by them on June 25, 2001. The mail log is attached as Exhibit D.
6. A final draft of the patent application was sent to me by email on July 27, 2001. A copy of the email letter accompanying the copy is attached as Exhibit E.
7. The patent application serial number 09/953,544, to which the instant patent application claims priority, was constructively reduced to practice by on September 17, 2001.
8. These exhibits show conception prior to the effective date of the reference plus diligence from prior to the reference date of Dec. 4, 2000 to constructive reduction to practice on September 17, 2001.

MEG00-009B

Serial no. 10/614,928

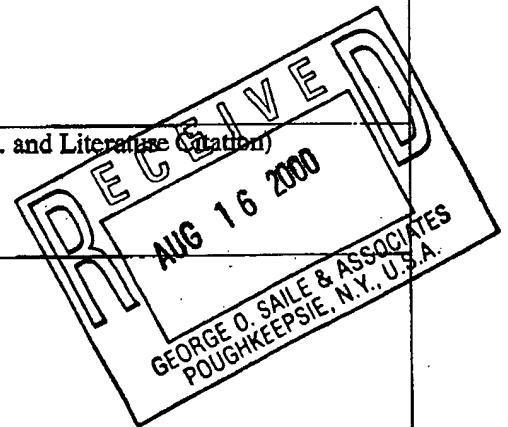
I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

<i>Jin-Yuan Lee</i>	<i>Jun-13, 2006</i>
Jin-yuan Lee	Date

Exhibit A

Invention Disclosure of Megic Corp. Page of Confidential (When Completed)

Full Name(s) of Inventor(s)		Employee No.	Department	Dept. Code	Tel No.	For Use by IP Law Disclosure No.
English	Chinese					
Jin-yuan Lee	李進源					2000-009
	林茂雄					Received Date: (Time Stamp)
<p>Title of Invention –</p> <ul style="list-style-type: none"> English: A structure of high performance combo chip and processing method Chinese: 						
<p>Background Information – Current Practice and Disadvantages</p> <p>Currently, high performance combo chip is in MCM (multiple chip module) or MCP (multiple chip package) format. The disadvantages of MCM and MCP are higher cost and bigger package size.</p>						
<p>Main Points of Claim (Please List Item by Item)</p> <ol style="list-style-type: none"> Combining multiple chips face to face I/Os of combo chip are ball grid array on the bottom of top chips. Wafer level processing 						
<p>Problem Solved or Improvements Obtained by this Invention (Please List Item by Item)</p> <ol style="list-style-type: none"> High performance system on chip can be achieved by combining multiple chips face to face. Smaller package size It can be Lower manufacturing cost because of wafer level processing 						
<p>Keyword Search for Patent/Literatures</p>						
<p>Patent/Literatures Search Result (Please Specify Similar Patent No. and Literature Citation)</p>						
<p>Detailed Description of Invention – (Continued Next Page)</p>						
<p>Witnesses: The Two Witnesses whose Signatures appear below have <u>Read</u> and <u>Understand</u> this Entire Invention Disclosure.</p> <p>Signature of Witness Date</p>		<p>Disclosure Submitted by</p>				
		Inventor's Signature Date		Inventor's Signature Date		
		Jin-Yuan Lee				
		Inventor's Signature Date		Inventor's Signature Date		
<p>J.J. Chan</p> <p>Signature of Witness Date</p>		<p>Manly Li</p>				
<p>K.H. Peng</p>						



Invention Disclosure of Megic Corp. Page of Confidential (When Completed)

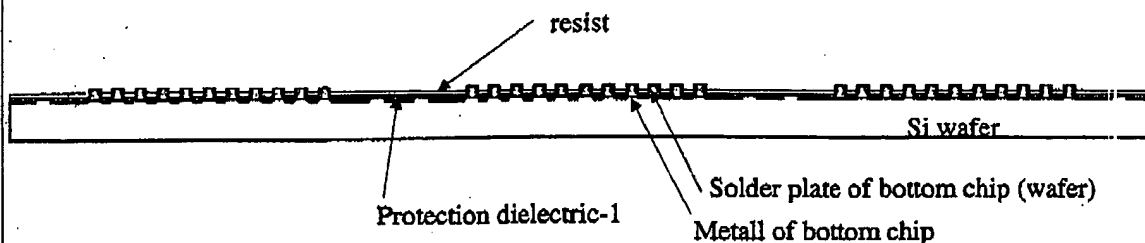
Detailed Description of Invention - Continued

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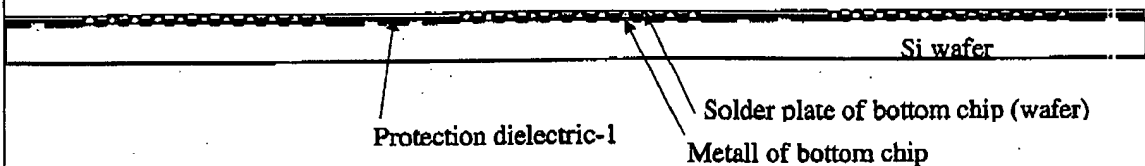
1. Solder plate formation:

- *. Solder plate formation by conventional plating.



2. Solder plate planarization:

- *. After plating of solder material, a solder plate planarization is performed by CMP process
- *. Resist stripping and seed metal etching



Witnesses: The Two Witnesses
whose Signatures appear below
have Read and Understand this
Entire Invention Disclosure.

Signature of Witness Date

J. J. Chan

Signature of Witness Date

K. H. Pang

Disclosure Submitted by

Inventor's Signature Date

Jin-Yuan Lee

Inventor's Signature Date

Inventor's Signature Date

Inventor's Signature Date

M. S. L.

Invention Disclosure of Megic Corp. Page 3 of 7 Confidential (When Completed)

Detailed Description of Invention - Continued

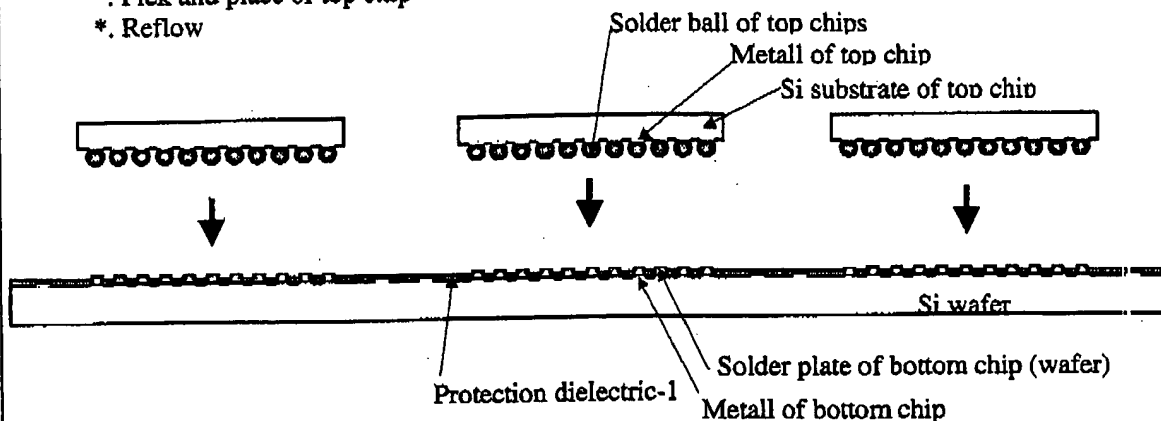
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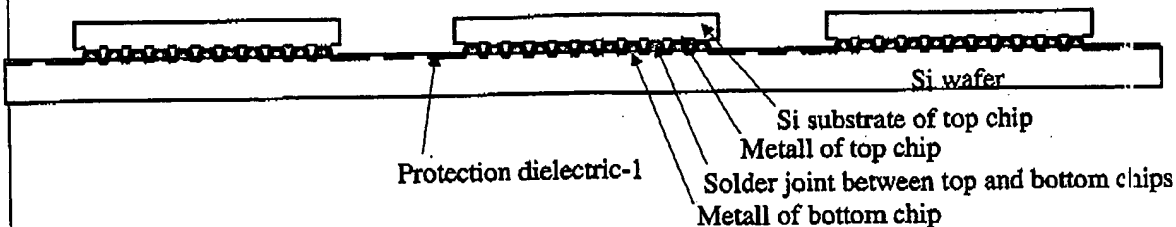
2000-009

3. Chip on wafer assembly-1

- *. Flux coating
- *. Pick and place of top chip
- *. Reflow



4. Clean after reflow



Witnesses: The Two Witnesses
whose Signatures appear below
have Read and Understand this
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Signature of Witness Date

J. J. Chan

Signature of Witness Date

K. H. Peng

Disclosure Submitted by

Inventor's Signature Date

Jin-Yuan Lee

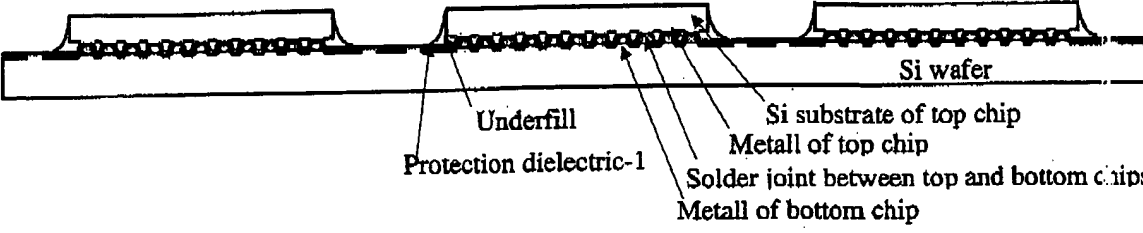
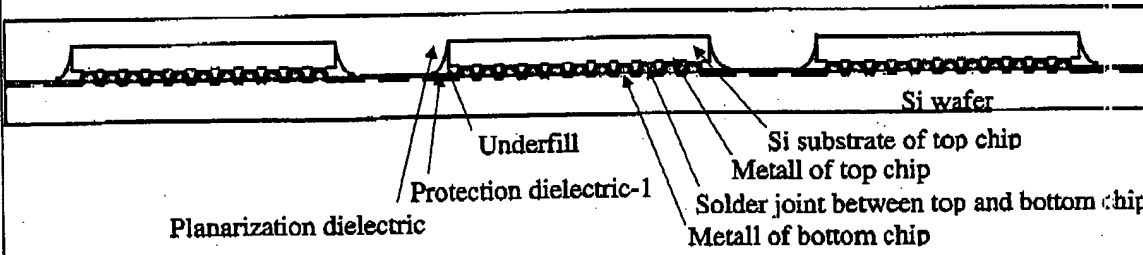
Inventor's Signature Date

Inventor's Signature Date

Inventor's Signature Date

Mou Shing Li

Invention Disclosure of Megic Corp. Page 4 of 7 Confidential (When Completed)

Detailed Description of Invention – Continued	For Use by IP Law Disclosure No. 2000-009	
<p>5. Under-fill</p> <p>*. Under-fill dispensation</p> <p>*. Curing</p> 		
<p>6. Planarization dielectric coating or lamination</p> 		
Witnesses: The Two Witnesses whose Signatures appear below have Read and Understand this Entire Invention Disclosure.	Disclosure Submitted by	
Signature of Witness Date	Inventor's Signature Date <i>Jin-Tuan Lee</i>	Inventor's Signature Date
<i>J.J. Chan</i> Signature of Witness Date	Inventor's Signature Date <i>Ming Shing L.</i>	Inventor's Signature Date
<i>H. H. Pang</i>		

Invention Disclosure of Megic Corp. Page 5 of 7 Confidential (When Completed)

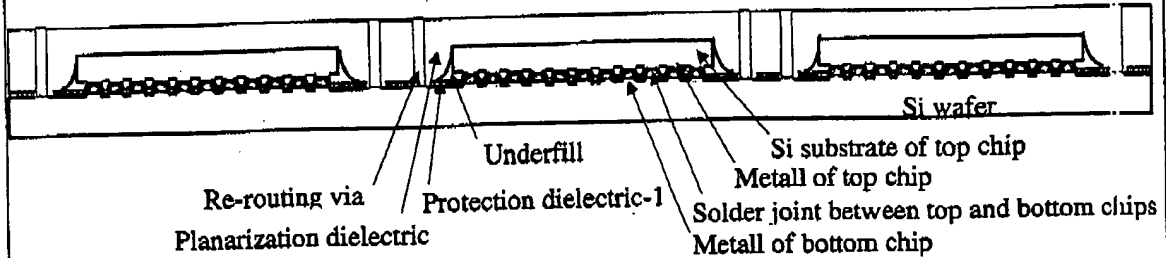
Detailed Description of Invention - Continued

For Use by IP Law
Disclosure No.

2000-009

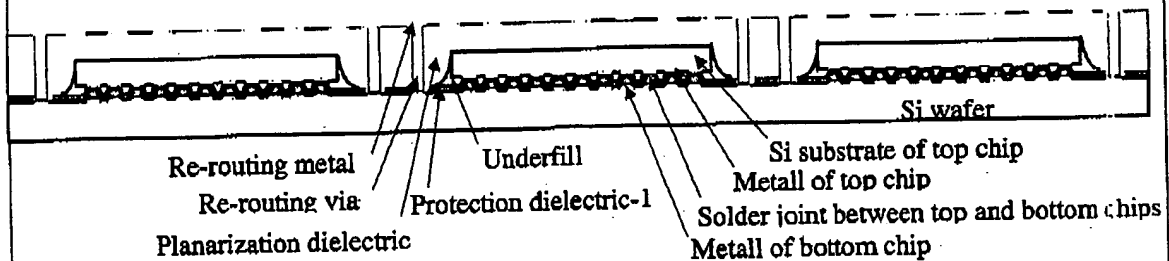
7. Re-routing via formation

- *. Via hole formation by laser drill or photo/development



8. Re-routing metal formation

- *. Seed metal sputtering
- *. Re-routing photo process
- *. Re-routing metal plating
- *. Resist stripping



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have Read and Understand this
Entire Invention Disclosure.

Signature of Witness Date

J. J. Chan

Signature of Witness Date

K. H. Peng

Disclosure Submitted by

Inventor's Signature Date

Jin-Tuan Lee

Inventor's Signature Date:

Inventor's Signature Date

Inventor's Signature Date:

Mandy Li

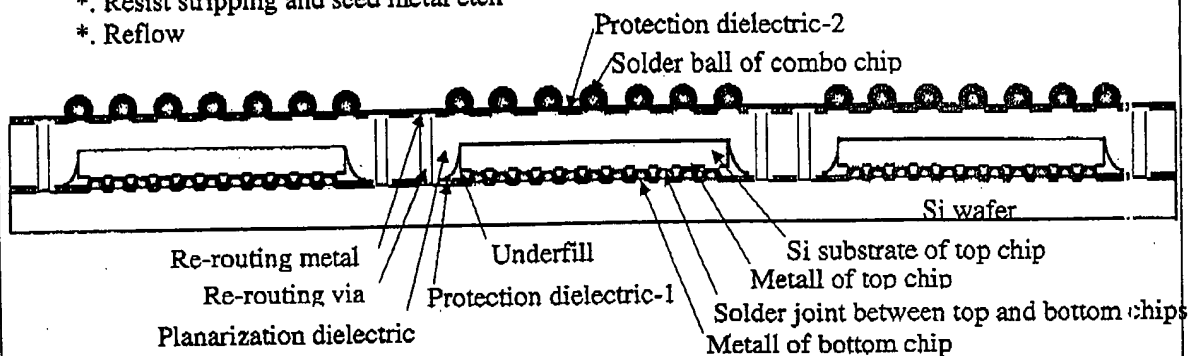
Detailed Description of Invention - Continued

For Use by IP Law
Disclosure No.

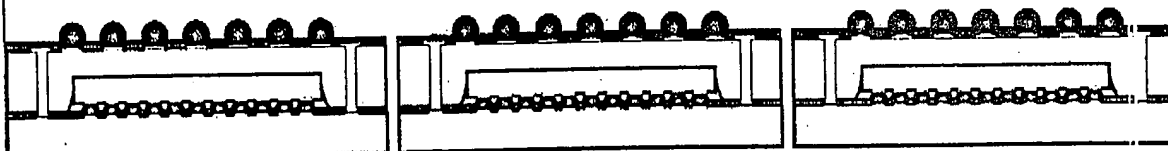
2000-009

9. Solder ball formation on combo chip

- *. Solder bump photo process
- *. Solder bump electro-plating
- *. Resist stripping and seed metal etch
- *. Reflow



10. Dice saw of combo chip



Witnesses: The Two Witnesses
whose Signatures appear below
have Read and Understand this
Entire Invention Disclosure.

Signature of Witness Date

J. J. Chan

Signature of Witness Date

K. H. Peng

Disclosure Submitted by

Inventor's Signature Date

Jin-Tuan Lee

Inventor's Signature Date

Inventor's Signature Date

Inventor's Signature Date

Mou Shing Li

Invention Disclosure of Megic Corp. Page 7 of 7 Confidential (When Completed)

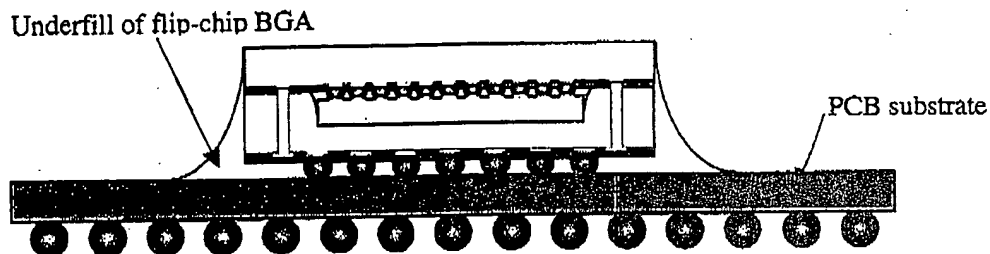
Detailed Description of Invention - Continued

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2000-009

11. Flip-chip BGA package formation

*. Combo chip BGA package performed by conventional flip-chip assembly



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whose Signatures appear below
have Read and Understand this
Entire Invention Disclosure.

Signature of Witness Date

J. J. Chan

Signature of Witness Date

K. H. Peng

Disclosure Submitted by

Inventor's Signature Date

Jin-Yuan Lee

Inventor's Signature Date

Inventor's Signature Date

Inventor's Signature Date

Mou Shing Li



Exhibit B
GEORGE O. SAILE & ASSOCIATES
20 MCINTOSH DRIVE
POUGHKEEPSIE, NY 12603

September 18, 2000

TO: M.S. Lin
MEGIC Corp.

FROM: Stephen B. Ackerman
Fax: 914 4712064

Subject: Patent Application Reference MEG 2000-009
Inventor: J.Y. Lee

Please have the Inventor review the enclosed Draft Patent Application. He should make any changes he sees fit, answer all of our questions, and fill in the blanks. The Declaration and Assignment are enclosed for his completion. Please complete the attached Small Entity Form. Review the Drawings carefully for any errors AND ADDITIONS. This is the time when we have the best opportunity to make the description of the invention complete and correct.

Please return the corrected description and Drawing as soon as you can.

With Best Regards,

Stephen B. Ackerman

[illegible]

Dockets Returned

[illegible]

Exhibit E

To: Chris Wang, Megic, INTERNET:chrishwang@megic.com.tw
From: Stephen Ackerman, 102706,1346
Date: 7/27/2001, 11:51 AM
Re: MEG00-009 and -010

Hi Chris,

Here are the final versions of the text of MEG00-009 and MEG00-010. Drawings and papers for signing are being sent separately by fax.

With best regards,
Steve